CLAIMS:

1.   Integrated circuit having a plurality of processing modules (M, S) and an
interconnect means (N) for coupling said plurality of processing modules (M, S) and for
enabling a device-level communication based on transactions between said plurality of
processing modules (M, S), wherein at least one first processing module (M) issues at least

5   one transaction towards at least one second processing module (S) comprising:
            at least one transaction abortion unit (TAU) for aborting at least one
transaction issued from said first module by receiving an abort request (abt) issued by said
first module (M), by initiating a discard of said at least one transaction to be aborted, and by
issuing a response (abt_ack) indicating the success/failure of the requested transaction

10   abortion.

2.   Integrated circuit according to claim 1, further comprising:
            at least one network interface (NI) associated to one of said plurality of
processing modules (M, S), for controlling the communication between said one of said

15   plurality of processing modules (M, S) and said interconnect (N),
            wherein said at least one transaction abortion unit (TAU) is arranged in one of
said network interfaces (NI).

3.   Integrated circuit according to claim 2, wherein

20   said at least one transaction abortion unit (TAU) is adapted to perform said at
least one transaction abortion atomically or partially.

4.   Integrated circuit according to claim 2, wherein
            said at least one network interface (NI) further comprise a request buffer

25   (REQ) for buffering received data,
            wherein said transaction abortion unit (TAU) is adapted to issue a discard for
said at least one transaction to be aborted as stored in said request buffer (REQ).

5.   Integrated circuit according to claim 2 or 4, wherein

said at least one network interface (NI) further comprise a response buffer
(RESP) for buffering outgoing data,

wherein said transaction abortion unit (TAU) is adapted to issue a discard for
5   said at least one transaction to be aborted as stored in said response buffer (RESP).

6.   Integrated circuit according to claim 1, wherein

said request for said at least one transaction abortion specifies which

transactions are to be aborted, and

10   said response (abt_ack) issued by said transaction abortion unit (TAU) specifies which of the

requested at least one transaction have been aborted.

7.   Method for transaction abortion in an integrated circuit having a plurality of

processing modules (M, S) and an interconnect means (N) for coupling said plurality of

15   processing modules (M, S) and for enabling a device-level communication based on

transactions between said plurality of processing modules (M, S), wherein at least one first

processing module (M) issues at least one transaction towards at least one second processing

module (S) comprising the step of:

aborting at least one transaction issued from said first module by receiving an

20   abort request (abt) issued by said first module (M), by initiating a discard of said at least one

transaction to be aborted, and by issuing a response (abt_ack) indicating the success/failure of

the requested transaction abortion.

8.   Data processing system, comprising a plurality of processing modules (M, S)

25   and an interconnect means (N) for coupling said plurality of processing modules (M, S) and

for enabling a device-level communication based on transactions between said plurality of

processing modules (M, S), wherein at least one first processing module (M) issues at least

one transaction towards at least one second processing module (S) comprising:

at least one transaction abortion unit (TAU) for aborting at least one

30   transaction issued from said first module by receiving an abort request (abt) issued by said

first module (M), by initiating a discard of said at least one transaction to be aborted, and by

issuing a response (abt_ack) indicating the success/failure of the requested transaction

abortion.